Q.P. Code: 20EC4209 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year II Semester Regular Examinations November-2021

FPGA ARCHITECTURE & APPLICATIONS

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Compare PLA, PAL and PLDs with respect to different features, programming and Applications.	L4	4M
	b	Explain and draw the architecture of lattice ISPLSI CPLD	L2	4M
	c	Implement the following Boolean function using PLA having 3 inputs, 3product terms and 2 outputs. $F_1(A,B,C) = AB\cdot C\cdot + A\,B\cdot C + ABC$ $F_2(A,B,C) = A\cdot B\,C + A\,B\cdot C + ABC$	L3	4M
		OR		
2	a	Draw the logic diagram of MAX 7000 CPLD macrocell and explain its Functioning.	L1	6M
	b	Explain the architecture of Altera Max 7000 series.	L2	6M

UNIT-II

3	a	Write about FPGA Programming Technologies in detail.	L1	6M
	b	Explain the functions of different blocks in Xilinx XC4000 CLB	L2	6M
		OR		
4	a	Draw the architecture of Altera flex 10000 FPGAs and Explain it	L1	4M
	b	List out the applications of FPGAs.	L4	8M

UNIT-III

5	a	Explain about FSM types, properties, design and applications.	L2	6M
	b	Explain the basic concepts of petrinets and state its properities.	L2	6M
		OR		
6	a	Illustrate about metastability characteristics.	L3	6M
	b	Discuss about Extended Petri nets for Parallel Controllers.	L2	6M

UNIT-IV

7	a	Design of the one to three pulse generator by using ROM.	L5	6M
	b	Design of a More Complex FSM by using a ROM as the PLD.	L5	6M
		OR		
8	a	List the state machine types.	L3	6M
	b	Discuss the device selection consideration.	L2	6M

UNIT-V

9	a	Design the CLB combinational circuit by using parallel adder cell.	L5	6M
	b	Design the combinational circuit by using parallel adder.	L5	6M
		OR		
10	a	Design the state machine for decade counter.	L5	6M
	b	Design the Schematic for full adder combinational circuit by using parallel adder cell.	L5	6M

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